Remarks:

Applicants (hereinafter, Applicant) hereby request reconsideration of the application.

Applicant acknowledges the Examiner's confirmation of receipt of the claim for priority and certified copy of the priority application under 35 U.S.C. § 119(a)-(d).

Claims 1 and 3-19 are now in the application. Claim 1 has been amended. No new matter is believed to have been added. Claim 2 has been cancelled without prejudice.

Claims 10-19 are *withdrawn from consideration*. Affirmation of the election is herewith made regarding item 1 on page 2 of the Office action.

In item 5 (on pages 2-3) of the Office action, claims 1, 3 and 9 have been rejected as being obvious over Arnold (U.S. Pat. No. 5,937,296) in view of Nishimura (U.S. Pat. No. 4,949,138) under 35 U.S.C. § 103.

In item 5 (on page 4) of the Office action, claim 2 has been rejected as being obvious over Arnold (U.S. Pat. No. 5,937,296) in view of Nishimura and Nitayama et al. (U.S. Pat.

No. 5,905,279) (hereinafter, "Nitayama") under 35 U.S.C. § 103.

In item 5 (on page 5) of the Office action, claims 4-8 have been rejected as being obvious over Arnold (U.S. Pat. No. 5,937,296) in view of Nishimura (U.S. Pat. No. 4,949,138) and Wallace et al. (U.S. Pat. No. 6,277,681) (hereinafter, "Wallace") under 35 U.S.C. § 103.

The rejections have been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found in original claim 2, Figs. 1 to 4 and Figs. 6 to 8 of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia, a trench capacitor, comprising:

said trench having an upper region and a lower region <u>and a conductive trench filling formed of tungsten-containing material disposed in said upper and lower regions of said trench;</u>

a buried well formed in said substrate, said lower region at least partly extending through said buried well; and

a dielectric layer of tungsten oxide for lining said lower region, said dielectric layer serving as a capacitor dielectric.

Accordingly, the *present invention is directed to* a trench capacitor formed in a substrate and a trench having an upper region and a lower region. An insulation collar is formed in the upper region of the trench. The lower region of the trench extends through a buried well. A dielectric layer, which is formed from tungsten oxide, serves as a capacitor dielectric. The invention further includes a conductive trench filling (which is disposed in the trench) formed of silicon or a tungsten-containing material. Figs. 1 to 4 and Figs. 6 to 8, show that the trench filling extends through the lower region and through the upper region, which is defined by the insulating collar.

The *Arnold* reference discloses a memory cell for a dynamic random access memory including a pass transistor and a storage capacitor. The transistor is a vertical transistor formed along an upper portion of a sidewall of a polysilicon-filled trench in a monocrystalline silicon body. The source and drain

are located in the body, and the source contact, gate and gate contact are located in the trench. The gate dielectric is formed as an oxide layer on the sidewall portion of the trench. The capacitor is a vertical capacitor formed along a deeper portion of the trench and has (as its storage plate) a lower polysilicon layer in the trench. The capacitor has (as its reference plate) a deep doped well in the body. The source contact and the storage plate are in electrical contact. The source contact and the gate contact are electrically isolated from one another.

The *Nishimura* reference discloses a semiconductor IC device having a memory cell. A word line is buried in a groove formed in a semiconductor layer, a transfer gate transistor is constructed by the word line and a side area thereof. A capacitor is formed on the surface of the semiconductor layer. The capacitor has an electrode as a source or a drain region of the transfer gate transistor. A dielectric film is in contact with the electrode.

In other words, the Nishimura reference teaches a trench capacitor having a lower region and an upper region. See Figs. 3A to 3J. The upper region is defined by a collar oxide 111. See Fig. 3B; column 4, line 14. In the lower region of the trench capacitor, a first doped polysilicon layer 105 is

covered by a tungsten silicide or tungsten nitride layer 107. The rest of the lower region of the trench is filled with doped polysilicon 109. See column 4, lines 3 to 8. The tungsten-containing layer 107 is a liner layer that extends only in the lower region of the trench. The upper region of the trench is filled with another silicon filling 113. See column 4, lines 20 to 22.

In contrast, the *present invention* is based on a different concept. Accordingly, the filling of the trench is defined to extend through the lower region and the upper region. The filling is formed of a tungsten-containing material.

Further, the *Nitayama* reference discloses a memory cell having a low storage node resistance and a method of manufacturing the same. A trench type memory cell (in addition to storage node polysilicon) has a conductive material embedded in the storage node. The conductive material may be WSi, TiSi, W, Ti, or TiN. The conductive material provides a low storage node resistance which facilitates the realization of 256 Mbit memory cells.

Accordingly, Nitayama does not teach using a tungsten-containing filling in the lower region and the upper region of the trench. Neither does the Wallace reference overcome the deficiencies of Arnold, Nishimura, and Nitayama.

Clearly, the references do not show "*said trench having an upper region and a lower region and a conductive trench filling formed of tungsten-containing material disposed in said upper and lower regions of said trench; a buried well formed in said substrate, said lower region at least partly extending through said buried well; and a dielectric layer of tungsten oxide for lining said lower region, said dielectric layer serving as a capacitor dielectric*", as recited in claim 1 of the instant application (emphasis added). Thus, neither can the specific combination of the aforementioned limitations be shown.

In view of the foregoing, reconsideration and allowance of claims 1 and 3-19 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, the Examiner is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and

Greenberg, P.A., No. 12-1099.

Respectfully submitted,

For Applicant

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

<u>In the claims:</u>

Claim 1 (amended). A trench capacitor, comprising:

a substrate formed with a trench;

said trench having an upper region and a lower region <u>and a conductive trench filling formed of tungsten-containing material disposed in said upper and lower regions of said trench;</u>

an insulation collar formed in said upper region;

a buried well formed in said substrate, said lower region at least partly extending through said buried well; <u>and</u>

a dielectric layer of tungsten oxide for lining said lower region, said dielectric layer serving as a capacitor dielectric[; and

[a conductive trench filling disposed in said trench].